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Sir:

Transmitted herewith for filing is a utility patent application of

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for: INTERCOM SYSTEM HAVING UNIFIED CONTROL AND AUDIO DATA TRANSPORT

ENCLOSED are the following:

1. ☒ Specification, abstract and claims of 23 Pages.
2. ☒ 7 sheets of ☒ formal ☐ informal drawings ☐ No drawings.
3. ☒ Declaration (original or copy) by the named inventor(s).
4. ☐ Preliminary Amendment
5. ☐ Information Disclosure Statement
6. ☐ Other:

NOTE the following:

7. ☐ Applicant is a small entity. Copy of Small Entity Statement enclosed – 50% Filing Fee Reduction (if applicable)
8. ☒ The prior application is assigned to Clear Com
9. This application is a:
   ☒ Continuation ☐ Divisional ☐ Continuation-in-Part (CIP) of Prior Application
   Serial No. 08/835,339
   Filed: April 7, 1997
10. ☐ Priority of the following application(s) is (are) claimed under 35 U.S.C. 119:

Serial No.	Date Filed	Country	Certified Copy of Priority Doc. Filed USSN or PCT#	Certified Copy of Priority Doc. Filed Date

11. ☐ An Extension of Time is filed concurrently herewith for the parent application.
12. ☐ Cancel claims _____ prior to calculation of the filing fee.

FILING FEE: calculated below (after accounting for any preliminary amendment or claims cancellations if noted above):

☒	Total Claims	2	Total Claims Subject to Fees: 0	$
☒	Independent Claims	2	Total Claims Subject to Fees:	$
☐	Multiple Dependent Claims			$
☒	Basic Filing Fee			$710.00
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Respectfully submitted,

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INTERCOM SYSTEM HAVING UNIFIED CONTROL AND AUDIO DATA TRANSPORT

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CROSS-REFERENCE TO RELATED APPLICATIONS AND COPYRIGHT NOTIFICATION

This application depends for priority upon U.S. Provisional Patent Application Ser. No. 60/042,965 filed on April 4, 1997, entitled INTERCOM SYSTEM HAVING UNIFIED CONTROL AND AUDIO DATA TRANSPORT, and is a Continuation of U.S. Patent Application Serial No. 08/835,339 entitled INTERCOM SYSTEM HAVING UNIFIED CONTROL AND AUDIO DATA TRANSPORT. A portion of the disclosure of the parent Provisional Patent Application contains material which is subject to copyright protection. The copyright owners have no objection to the facsimile reproduction, by anyone, of the patent document or the patent disclosure as it appears in the patent and trademark office patent file or records, but otherwise reserve all copyright rights whatsoever.

FIELD OF THE INVENTION

The invention relates generally to multi-user intercom systems and, more specifically, to an intercom system providing a fail-safe, redundant and scaleable architecture implemented with digital Time Division Multiplexing technology for integrated audio and control data transport.

BACKGROUND OF THE INVENTION

Intercom systems provide communication between two or more remotely located individuals. More advanced intercom systems provide conference-type communication, simultaneously connecting several intercom stations so that several individuals can communicate with groups and sub-groups of other system users.

Conventional conference-type intercom systems include a switch matrix, commonly referred to as a crosspoint switch, which allows any user to communicate with any selectable mix of the remainder of the users. Crosspoint switches are normally used instead of direct point-to-point connections between source and destination equipment for all but the smallest implementations. A thorough discussion of prior art crosspoint switching schemes can be found in U.S. Patent No. 5,483,528 to Christensen, incorporated herein in its entirety by reference.

With crosspoint switches, all stations are connected directly to the crosspoint switch matrix which makes connections between the sources and destinations internally. In order to accommodate large numbers of switched audio channels, intercom systems typically distribute the crosspoint matrix across a number of bussed circuit modules or cards. Each module typically controls switch closures for connecting audio to or from a small group of intercom stations for which it is responsible. Each module typically employs a small local computer whose duties include, but are not limited to:

(a) Making and breaking audio crosspoint closures;

(b) Data communications with those intercom stations connected to it;

(c) Data communications with other matrix modules via a central data communications controller.

A significant disadvantage of crosspoint switches is the geometrically increasing size and cost of the switch matrix relative to the number of intercom users to be interconnected. For example, although a four station matrix requires only 16 switches and an interconnect backplane containing 4 circuit paths, a 100 station matrix requires 10,000 switches and dedication of 100 backplane circuit paths. Thus the available matrix-of-switches crosspoint topology is practical only for relatively small systems.

Noise considerations also become more important as matrix-switch-based intercom systems grow in size. Resistive summing of multiple analog sources into a common destination results in signal-to-noise degradation. Driving multiple destinations from a single source requires the addition of analog buffers to meet impedance-matching fanout requirements. These buffers also degrade signal-to-noise performance.

Partially addressing these problems, the Christensen patent discloses a system which interconnects intercom stations, making use of Time Division Multiplexing (TDM). In this system, multiple audio signal sources (stations) are periodically sampled and digitized at a high frequency and interleaved cyclically onto a parallel bus. At each destination (station) on the bus, a receiver picks from the data stream the digitized samples associated with a given source or combination of sources. It converts these signals to analog voltages and reconstructs the original analog waveform or combination of waveforms by interpolating (integrating) between the sequential samples taken from the bus.

Although TDM greatly improves the efficiency of audio transport in intercom systems, traditional intercom systems (even the system disclosed in Christensen) suffer limitations in the transport of the large volume of control data upon which intercom system operation depends. Consider, for example, the requirement for any practical intercom system, that an audio connection be established very quickly, and usually bi-directionally. Control messages must

pass between intercom stations over narrow bandwidth data channels, separate from the audio channel, typically through an intermediary or central data communications controller to establish the audio connection. The station initiating the conversation must notify the second station, through the intermediary, that it desires to establish a talk-listen connection. The second station then acknowledges the first station's request and replies with a request to establish its own talk-listen connection, also through the intermediary processor. As system complexity and size increase, the number of messages passed between stations escalates, and the limited bandwidth of the data links, especially when implemented as serial data channels, tends to become a bottleneck for data flow. If the intermediary processor and its communications links delay the control message-passing to any great degree, the delay can become objectionable to users of the intercom. The party attempting to initiate a conversation may begin to speak before the link is established, causing the second party to receive a truncated, unintelligible message. The common intercom topology employing serial control communications through an intermediary processor, even including TDM-based audio signal transport, can be overwhelmed by the volume of data transactions when an intercom system reaches a critical size.

Also, if the central communications processor malfunctions, the capacity for data communication is lost and cannot be reestablished until the central processor is repaired or replaced. Avoiding this failure mode by using redundant central communications processors tends to be awkward and complicated.

An additional flaw in some available systems can be found in the use of the TDM bus for transport of mixed and attenuated audio signals. This redundant use of the TDM bus narrows the available bandwidth for more critical primary audio transport between stations and would preferably be avoided.

Therefore, as demand grows for ever larger intercom systems, the industry needs a mechanism which provides wider bandwidth data communications to support the increased channel capacity of TDM audio transports. Preferably such a system would provide immunity from catastrophic single-point failure without the appreciable complexity of redundant central data communications processors.

SUMMARY OF THE INVENTION

To address the shortcomings of available crosspoint-based and TDM-based intercom systems which use a central communications and control processor as an intermediary in the transport of control signals between intercom stations, the present invention provides a network of peer processor-controlled circuit modules comprising a plurality of processor circuit modules connected to a common, time-division-multiplexed (TDM) bus, wherein bandwidth on the TDM bus is shared between a digital audio data transport and an inter-processor control message.

In a preferred embodiment, each of the processor circuit modules includes a control data communications circuit (CDCC) functioning as a communications co-processor and comprising means for automating the transmission and reception of simultaneous variable-length control messages among any number of the peer processor-controlled circuit modules using the TDM parallel bus, means for interleaving the control message with the audio data on the TDM parallel bus, and means for distributing the audio data and control data to a plurality of peripheral equipment stations capable of generating and receiving audio and control data. Means for providing automatic notification at every processor-controlled circuit module on the network when any other processor-controlled circuit module connects to or disconnects from the network is also provided for more rapid inter-processor communication

Although the modularity of this system may appear similar to available system designs with respect to the fact that interconnected circuit modules each manage traffic to and from groups of peripheral stations (such as intercoms), a fundamental distinction exists between this implementation and those available, in that no central intermediary or processor controls the overall system operation nor does any single processor or intermediary control data communications among modules. The invention provides vastly increased data communications bandwidth over the serial implementations previously employed by intercom systems, and

eliminates the risks of central processor failure in establishing and maintaining audio paths. This new intercom system includes an audio signal attenuation and mixing scheme which does not require mixed signals to re-enter the bus after attenuation and mixing is complete, thereby allowing additional bandwidth for control and audio data transfer among intercom stations. A primary advantage of the present invention is the high speed of control data transport among the modules, as compared with existing serial data communications implementations employed in existing intercoms.

Another advantage of the present invention is the economy of shared hardware resources which manage both audio transport and data communications.

Another advantage of the present invention is the safety from catastrophic single-point failure previously associated with a hierarchical communications scheme, i.e. a single central communications and control processor over multiple slave controllers.

Still another advantage of the present invention is the small size of the system hardware.

Still another advantage of the present invention is the bus-independent attenuation and mixing scheme provided.

Still another advantage of the present invention is the re-configurability of the intercom system layout and features.

Yet another advantage of the present invention is the scaleable nature of the provided architecture, providing the ability to interconnect over a thousand stations on a single distributed system.

Another advantage of the present invention is the ability to integrate available digital phone line technology to provide a geographically distributed, reliable intercom system to a large group of users.

BRIEF DESCRIPTION OF THE DRAWINGS

The aforementioned advantages of the present invention as well as additional advantages thereof will be more clearly understood hereinafter as a result of a detailed description of a preferred embodiment of the invention when taken in conjunction with the following drawings in which:

FIG. 1 is a simplified block diagram of the intercom system of the present invention;

FIG. 2 is a block diagram of a Matrix Card used in the intercom system of the present invention;

FIG. 3 is a block diagram of a Configuration Card used in the intercom system of the present invention;

FIG. 4 is a diagram of that portion of dual-port RAM used to provide data queues in conjunction with the CDCC described below, in the intercom system of the present invention, wherein lines 132, 134, and 136 provide interconnect to the CDCC block illustrated in FIG. 5;

FIG. 5 is a block diagram of the preferred Control Data Communications Circuit (CDCC) employed on the Configuration Card of FIG. 2 and the Matrix Card of FIG. 2, wherein lines 132-138 provide interconnect to the dual-port RAM portion illustrated in FIG. 4 and other resources on the Matrix Card illustrated in FIG. 2;

FIG. 6 illustrates the manner in which Audio Data transport and Control Data Communication share the TDM Time Frame in the system of the present invention;

FIG. 7 is a block diagram illustrating a preferred hardware audio circuit implemented in an application specific integrated circuit on the Matrix Card of FIG. 2;

FIG. 8 illustrates a scaled architecture including a plurality of systems illustrated in FIG. 1 interconnected to create a system having far greater user capacity while maintaining optimal audio bandwidth.

DETAILED DESCRIPTION OF THE DRAWINGS

FIG. 1 provides a system-level block diagram of the intercom of the present invention. TDM Data Bus 160 and TDM Control Bus 158 interconnect the cards in the intercom system matrix rack. Sixteen-bit-wide TDM Data Bus 160 provides transport for audio among all Matrix Cards 2 and provides inter-processor communication among all Matrix Cards 2 and the Configuration Card 4. The only system card not attached to the TDM Data Bus 160 is the primary clock card 8 which possesses neither intelligence nor communications capability.

TDM Control Bus 158 provides system-wide synchronized timing signals to all cards 2 and 4, thereby providing the foundation for data flow across TDM bus 160. TDM Control Bus 158 consists of Primary and Secondary (Backup) Clock Groups, generated respectively on the Primary Clock Card 8 and the Configuration Card 4. Circuitry on the Configuration Card 4 continuously monitors the quality of signals in the Primary and Secondary Clock Groups and arbitrates system use of these signals.

The presently preferred embodiment of the intercom system includes as many as twenty-five Matrix Cards 2 and two hundred intercom stations 6, although a plurality of systems may be linked, resulting in a much larger overall count of interconnected stations, in a manner discussed below. The system illustrated in FIG. 1 includes "N" Matrix Cards 2, numbered for reference from # 1 to #N. Eight intercom stations 6 may be connected to each Matrix Card 2 in the presently preferred embodiment, but more may be accommodated in a manner depending upon packaging constraints. It should be noted that stations 6 are denoted as intercoms because these are anticipated as the most common audio and data peripheral equipment to be used within the inventive system. However, any audio and/or data generating and/or receiving peripheral may be used, e.g., telephones, control equipment, and satellite link-up equipment.

The Primary Clock Card 8 is the source of Primary TDM Clock and Synchronization signals which are broadcast to all other cards in the system over the TDM Control Bus 158. Configuration computer 70 is connected to Configuration Card 4 via an RS-232, Ethernet, or compatible local connecting mechanism, providing a friendly interface to an intercom system user for modifying system configuration and events.

FIG. 2 provides a block diagram illustrating relevant features of Matrix Card 2. Control Application Specific Integrated Circuit (ASIC) 10 and Audio ASICs 140 are preferably very large gate arrays or field programmable gate arrays (FPGAs), but possibly any other device(s) of sufficient density and possessing a definable internal architecture. Taken together as a subsystem, these ASICs provide the core functions required of a Matrix Card 2, providing the audio and control data interface between eight intercom stations 6 and the TDM bus 160. As similar control ASIC 610 resides on the Configuration Card 4, as shown in FIG. 3.

Referring to FIGS. 2 and 3, on both cards 2 and 4 non-volatile ROM blocks 202 provide the code memory for a local microprocessor 30 and preferably comprises a flash-type memory to allow remote code revision without memory device replacement. At system power-up, or whenever a new Matrix Card 2 is hot-patched into a system under power, Matrix Card configuration information is loaded into a configuration data volatile memory 204 (RAM) on Matrix Card 2 Configuration Card 4. The loaded data describes for example, the function and electronic labeling of distinct switches at intercom stations 6 connected to the newly connected or newly powered-up Matrix Card 2, and the groupings of intercom stations 6 throughout the system for ease of use by a plurality of users each having different communications needs for the system. Control ASIC 10 implements the main interface and processing circuitry for audio and control data flow between the Matrix Card 2 and the remainder of the system, including audio ASIC interface block 211, CODEC timing block 212, frame and station service request block 213, I/O decode block 214, Control Data Communications Circuit (CDCC) block 100, data

routing block 216, and dual-port RAM address control timing block 217. A detailed block illustration of preferred Control Data Communications Circuit (CDCC) 100, used on Matrix Card 2 and Configuration Card 4, and implemented in control ASICs 10 and 610 (along with additional circuitry not shown) is shown in FIG. 5. Other circuitry, some of which is common to all types of embedded control applications, needs no further amplification here.

Configuration Card 4 provides several important system functions, but is preferably neither a repository of central control nor an arbiter of communications over other system cards. Its primary functions are to:

(a) provide (preferably multiple sets of) globally accessible configuration data for all system parameters;

(b) provide Secondary Clock Group signal generation

(c) monitor Primary and Secondary Clock Group signal quality

(d) dictate system-wide choice of Primary or Secondary Clock Group signals;

(e) communicate with Configuration PC 70 to acquire new system configuration data and log system events;

(f) provide miscellaneous system monitoring functions, such as temperature measurement and alarm monitoring;

(g) provide real-time clock maintenance by utilizing clock arbitration block 218 and clock generation block 219 in combination with reference clock 220.

The reader should note that Configuration Card 4 need not be present in an operating intercom system to send audio or control messages from one Matrix Card 2 to another. The intercom system will continue to operate without any interruption in audio transport or

interruption in the capacity to make and break connections between stations even if the Configuration Card 4 is unplugged during system operation.

As the Control Data Communication Circuit (CDCC) 100 in Control ASICs 10 and 610 is common to the core logic on the Matrix Card 2 and the Configuration Card 4, we will begin with a discussion of this important topic.

Referring to FIG. 5, fundamental to the present invention's inter-card data communications is the Control Data Communications Circuit (CDCC) 100. CDCC 100 resides in the control ASICs 10 and 610 on all Matrix 2 and Configuration 4 Cards, respectively. Both Matrix Card 2 and Configuration Card 4 will be collectively referred to as "cards" for the remainder of this discussion, since for the purposes of this discussion the CDCCs on both card types possess, by design, much of the same hardware, are driven by similar communications software, and exhibit substantially identical behavior. CDCC 100 automates multiple variable-length block data transfers simultaneously among any number of these cards on the TDM Data Bus 160, thereby relieving the system of the requirement for a centralized, intermediary processor. CDCC 100 comprises transmitter and receiver sections which interface to a single source (transmit) queue 205 in dual-port RAM 20 local to the same card and a plurality of destination (receive) queues 210, also in dual-port RAM 20.

As a control-message source, the transmit portion of each CDCC 100 in the intercom system may specify either a unique destination card receiver (which may even be the receiver on the transmitting card itself) or a global (multi-card) destination for a given message. The receiver portion of each CDCC 100 automatically acquires all control-messages for which it is the intended recipient, even when a plurality of cards simultaneously send it messages. This network implementation results in the transport of multiple simultaneous control messages without contention for hardware resources unlike existing serial communications

implementations. The intercom incurs no software arbitration overhead since the protocol is almost entirely implemented in hardware; the CDCC receiver portion is not overloaded even if it simultaneously receives control-messages from every card in the intercom system since it has a separate receive queue 210 for each possible message source.

A CDCC 100 manages the movement of blocks of data among multiple cards 2 and 4 using a portion of the bandwidth (refer to FIG. 6) of the TDM Data Bus 160. Each CDCC contains transmitter and receiver components whose common timing elements are synchronized by TDM frame synchronizing signals. (For the sake of brevity, source and destination components of CDCCs will be referred to as labeled in FIG. 5; the reader should understand that source and destination components are included on all CDCCs.)

In moving variable-length data blocks, each card's local microprocessor 30 and the CDCC 100 both access data queues from opposite sides of shared dual-port RAM 20. In sending a message, the microprocessor 30 stores data to a transmit (XMIT) queue 205. The CDCC transmitter automatically reads queue 205 and dispatches appropriately-timed data onto TDM bus 160 from it. Upon completion, the CDCC 100 transmitter portion interrupts the source card microprocessor 30 to indicate the availability of transmit queue 205 for the next message. CDCC receiver circuitry at the destination card automatically recognizes all data for which it is the intended recipient and places each incoming TDM datum into the receive queue 210 in dual-port RAM 20 associated with the address of the transmitting CDCC. After receiving a complete message, the destination CDCC interrupts its local microprocessor 30, which reads an internal register in the CDCC indicating which receive queue(s) contain(s) the new message(s).

Describing the process of sending a control message to a destination card in greater detail, the microprocessor 30 at the source card 2 or 4 performs three steps : First, the microprocessor 30 loads a variable-length message into the region in the dual-port RAM 20

reserved to hold the CDCC's transmit queue 205, and retains the location of the last message word (offset address from start-of-queue) through the second step, below; Second, the source microprocessor 30 writes the destination card's identity (address) in its Destination Address Register 110; Third, the source microprocessor 30 establishes the size of the variable-length message to be sent by specifying to its CDCC transmitter the location of the highest numbered data word in its transmit queue 205. This third step is accomplished by loading the offset of the last message word (retained from the first step, above) into its CDCC's Word-In-Queue Register 112. The CDCC's transmit hardware portion offsets the base address of its transmit queue 205 with the Word-In-Queue Register 112 and uses that combined address to fetch the (highest-numbered) first word of the message from its own transmit queue 205 in dual-port RAM 20. As the message is sent, the Word-In-Queue is regenerated at the receiver (described below) and the receiver uses this address offset to place the message data into the same-numbered location(s) in its receive queue 210. In loading its Word-In-Queue Register 112, the source microprocessor 30 triggers the process whereby the CDCC 100 transmit hardware portion automatically dispatches the message, one word per TDM frame, onto TDM bus 160 without further microprocessor 30 intervention. CDCC 100 transmitter hardware portion then concatenates the address byte from the destination CDCC's Address Register 110 with the Word-In-Queue Register 112 to form a Composite Destination Address Word 163, which is broadcast on TDM data bus 160 during the first time-slot of the time-slot pair assigned to the source card (based on the card's system address). Reference to FIG. 6, below, provides slot-pair structure details.

During each TDM frame, each CDCC 100 drives the TDM bus 160 during a particular, pre-designated time-slot pair determined by the source microprocessor's unique system address stored at register 133. As illustrated in FIG. 6, the first time-slot within the slot pair contains the source CDCC's Composite Destination Address Word 163, which includes both the Destination Card Address in the high byte 162 of the Composite Destination Address Word 163 and the

Word-In-Queue address at low byte 164 of the Composite Destination Address Word 163. During the second time-slot of the pair, designated the Control Data Word Time-Slot 166, the source CDCC places a control data word from it's transmit queue 205 onto TDM bus 160. Down-counter 114 automatically decrements Word-In-Queue Register 112 as each successive word of control data is transmitted. After sending the last word of the control message, in successive data frames, the source CDCC recognizes that Word-In-Queue Register 112 has decremented through zero and generates an interrupt (IRQ) to notify its microprocessor 30 that its transmit queue 205 is empty and available for the next message.

After transmit queue 205 is emptied, and until local microprocessor 30 gives the CDCC 100 transmitter hardware portion new data to transmit along with a new destination address, the CDCC transmitter hardware portion remains in an Idle state. While Idle, the CDCC transmitter hardware portion continues to drive TDM bus 160 within its assigned time-slot pair with a Composite Destination Address Word 163 that points to a non-existent destination card, but identifies this CDCC's card 2 or 4 as active in the intercom system. In fact, each card active on the intercom system's peer network transmits a Composite Destination Address Word 163 during the first time-slot of the time-slot pair assigned to that card on the basis of its unique system address, without regard to whether it is in an Idle state. The contents of this word is always distinguishable from the state of the undriven bus; every card's CDCC-100 receiver hardware portion inspects the contents of TDM bus 160 during all such time-slots and thereby determines which other cards 2 or 4 are connected to the network without polling the network for resident cards. The inventive CDCC 100 takes advantage of this fact by mapping the connection state of each card in the system to a bit in the multiple-word Card Population Register 120. Each card's CDCC provides additional circuitry which detects changes in the connection status of cards and generates a microprocessor 30 interrupt (IRQ) when any card joins or leaves the intercom system.

When the hardware receiver portion at the destination CDCC 100 recognizes its own address in the Destination CDCC Address field of a Composite Destination Address Word 163 at comparator 140, or recognizes a global message address at comparator 141, it accepts the word placed in the next time-slot on the TDM bus as message data intended for itself The CDCC's Receiver Address Generator 142 determines which receive queue 210 will receive the new data, having derived the address of the source from observation of the time-slot during which the matching Composite Destination Address Word 163 was received. Data received from card 1 is routed to queue 1, etc. The receiver CDCC places the data in a location in that queue specified by the Destination Word-In-Queue field of the Composite Destination Address Word 163. For example, data received from the source card's transmit queue 205 word number 17 is routed to the appropriate receive queue 210 word number 17, etc. When the destination CDCC recognizes that the incoming Word-In-Queue field has finally decremented to zero, indicating the reception of the last data word, it interrupts its local microprocessor 30, and indicates by means of the Frame and Station Service Request block 213 which receive queue 210 contains the new message.

Turning next to the manipulation of audio signals and referring to FIG. 2, the Matrix Card 2 core logic subsystem acquires, from the encoder sections of serial CODECs 50, bit streams representing audio signals from each of the intercom stations connected to its Matrix Card 2. It should be noted that the preferred system includes a single, dual-use CODEC 50 for every two intercom stations 6. The core logic synchronously converts this audio signal data to a form which it places on TDM bus 160 during a specific group of audio time-slots, based on the card's physical location (address) in the intercom rack, as illustrated in FIG. 6. Each card in turn places its group of digitized audio samples onto the TDM bus. From these data, all cards can sample any of two hundred channels of interest in a fully populated system.

The Matrix Card 2 core logic subsystem connects audio sources on TDM bus 160 to each of eight local station destinations 6, as if connected through a crosspoint switch. However, in this implementation the "switch" possesses faders (not shown) at the input to every crosspoint, a concept termed Variable Listen Levels. In other words, the core logic of Matrix Card 2 enables each destination station 6 to receive audio from any conceivable mix of the stations which communicate through the Matrix Cards 2 in the intercom system to TDM bus 160, as if connected by a crosspoint switch. However, by means of Variable Listen Levels in the current invention, each station's audio contribution can be individually adjusted relative to that of the other stations in the mix. This feature is useful in establishing a hierarchy of users, where some important user, perhaps a director or producer, needs to be monitored at a higher level than other audio sources, yet not completely kill the other sources in the mix. An intercom user may also employ Variable Listen Levels to boost the level of a soft speaker (or attenuate a loud one) relative to other users of the intercom, by means of depressing a key (not shown) on intercom station 6. Variable Listen Levels enables the current invention to provide a unique related feature, called Psycho-acoustic Level Control. This term applies to the situation in which the user of an intercom who wishes to boost the level of a particular station eventually runs out of gain because of an exceptionally weak audio signal on the channel of interest. In the current invention, when no additional boost is available to listen to a particular channel, successive key-presses intended to raise the volume of a desired signal instead automatically attenuate the other signals in the mix. This gives the user the impression of increasing the loudness for the channel of interest. To accomplish this mixing of audio with Variable Listen Levels, the core logic of Matrix Card 2 possesses eight identical audio acquisition circuits providing audio to a destination station connected to a Matrix Card 2 (refer to FIGS. 2, 6, and 7). Circuitry in the Control ASIC 10 portion of the core logic simultaneously fetches an audio sample from the TDM bus and attenuation data from dual-port RAM 20, during each of the two hundred audio data slot-times in the TDM frame illustrated in FIG. 6. The attenuation data across lines 704 and audio sample across lines 706 meet at an attenuator circuit 702 shown in FIG. 7, where the

attenuation data effectively provides the connection for a particular channel of audio data to the destination station, as follows: If the attenuation data indicates infinite attenuation, the TDM data from that source station is not connected to the destination station; if the attenuation data indicates no attenuation, then the station currently being sampled is mixed in at full volume; other attenuation values provide for variable amounts of the source signal to be passed into the mix of signals. After attenuation, whatever remains of a station's audio sample next passes to an accumulator 708 which arithmetically sums two-hundred sequential values at its input. Most of these values are zero under normal circumstances, since the user rarely desires to simultaneously listen to two-hundred stations. Attenuator 702 provides several bits of headroom to allow for the occurrence of out-of-range sums without numeric wrap-around. Clipper 710 cleanly removes these bits. The bulk of the remainder of the logic relating to the audio deals with synchronizing the serial interlaced bit streams from the audio CODECs 50 with the ongoing TDM activity.

Referring next to FIG. 8, a large-scale system architecture is provided, comprising a plurality of the systems 1 shown in FIG. 1 interconnected either locally or across long distance spans using digital telephone line connections, such as T-1 telephone lines. The plurality of systems are preferably interconnected by substituting a system interconnect card 11 for one Matrix Card 2 in a central system. Instead of connecting to up to eight intercom stations 6 (as would a Matrix Card 2), interconnect card 11 connects to up to eight additional intercom systems 1, each potentially having its own interconnect card 11 which may connect to still additional systems 1. While interconnect cards 11 are very similar to Matrix Cards 2 described above, there are minor distinctions intended to deal with system addressing which will be understood by those skilled in the art to which the present invention pertains.

While the present invention has been described with reference to certain preferred embodiments, those skilled in the art will recognize that various modifications and other embodiments may be provided. These other embodiments are intended to fall within the scope

of the present invention. For example, larger system bus widths may be utilized to increase system throughput and are clearly within the scope and spirit of this description. Similarly, alterations may be made to the layout of CDCC 100 without sacrificing the ability to transport control data from peer to peer in the intercom system without utilizing a single intermediary processor. In addition, the control data transport mechanism of the described intercom system may be incorporated into other electronic systems wherein high speed control communication is desired or necessary. Accordingly, all such modifications and additions are deemed to be within the scope of the invention which is to be limited only by the claims appended hereto.

CLAIMS

What is claimed is:

1. An intercom system for transferring audio information and data information among a plurality of users, the intercom system comprising:

a common, time-division-multiplexed parallel bus;

a plurality of circuit modules connected to the bus, each one of the circuit modules being connected to at least one peripheral station for control message and audio data interface between the peripheral stations and the bus;

each circuit module having a control data communication circuit having a receiver and a transmitter, the transmitter having assigned transmit time slots for transferring control messages onto the bus, the transmitter being configured for transmitting, in successive time slots, data identifying a unique address, each receiver being configured for distinguishing the address data received on the bus during a designated receive time slot for automatically determining which of the circuit modules is a source of a control message datum.

2. An intercom system for transferring audio information and data information among a plurality of users, the intercom system comprising:

a common, time-division-multiplexed parallel bus;

a plurality of matrix cards connected to the bus, each matrix card having at least one intercom station connected to it for audio and control data interface between the stations and the bus;

each matrix card having a control data communication circuit having a receiver and a transmitter, the transmitter having assigned transmit time slots for transferring data onto the bus, the transmitter being configured for transmitting; in successive time slots, data identifying a unique address, each receiver being configured for distinguishing the address data received on the bus during a designated receive time slot for automatically determining which matrix cards are connected to the bus.

INTERCOM SYSTEM HAVING UNIFIED CONTROL AND AUDIO DATA TRANSPORT

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John Franklin Anthony Jurrius
Lewis Clark McCoy

ABSTRACT

An intercom system utilizing peer-to-peer computer network hardware that shares bandwidth between digital audio transport and inter-processor data communications on a common time-division-multiplexed (TDM) parallel bus. The system hardware automates symmetric, simultaneous, variable-length data block transfers among all of the microprocessor-controlled cards in the system. These cards communicate without intervention by or assistance from a central controller or intermediary communications processor, thereby improving system throughput and reliability and decreasing system complexity. An additional benefit of the communication scheme employed herein is that all system cards automatically track changes in the population of other cards in the system. The intercom system described employs a Configuration Card connected to a configuration computer to provides the system supervisor with the ability to quickly configure the system for a particular use without altering the system's hardware configuration.

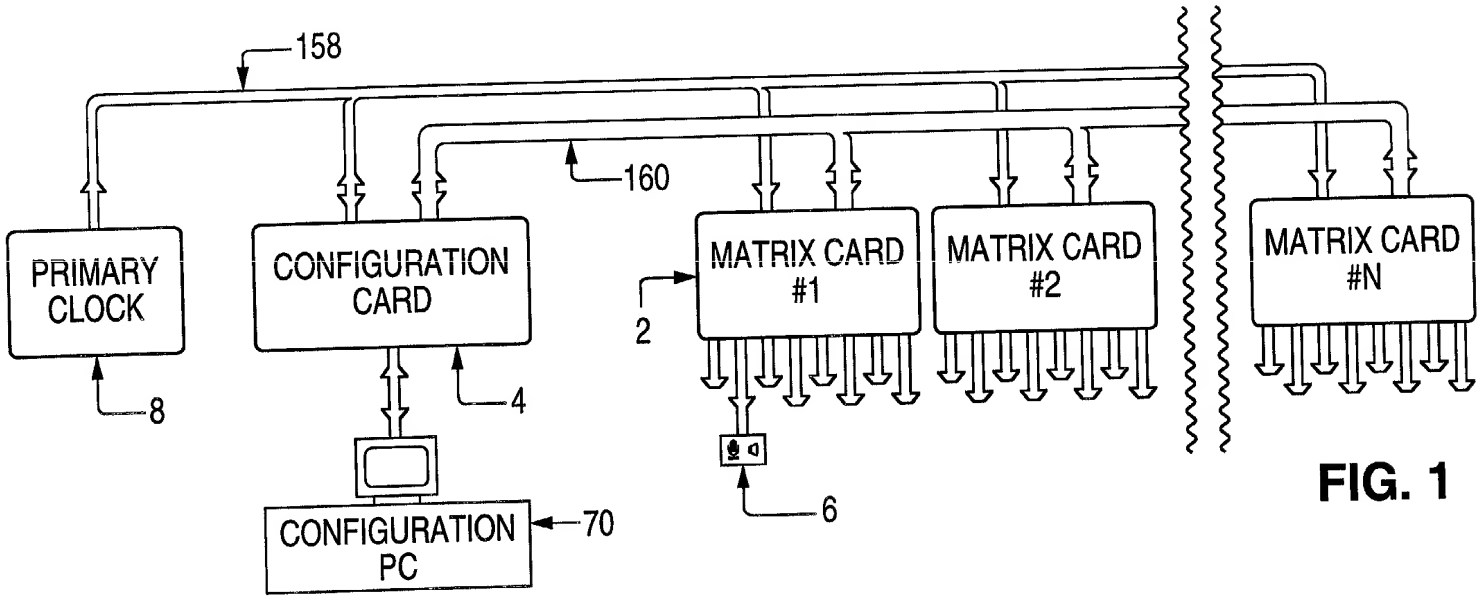
158
160
PRIMARY CLOCK
CONFIGURATION CARD
MATRIX CARD #1
MATRIX CARD #2
MATRIX CARD #N
2
8
4
6
CONFIGURATION PC
70

FIG. 1

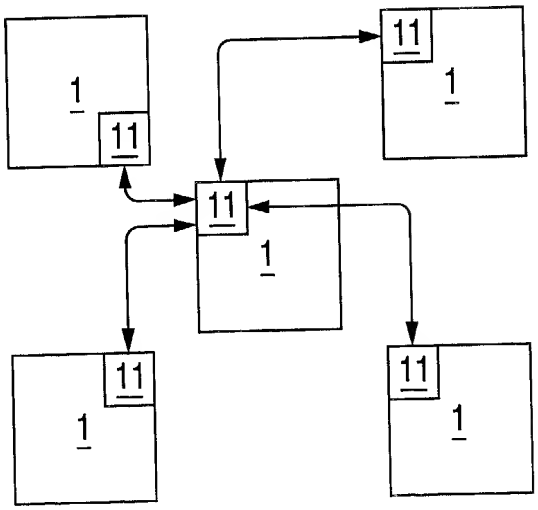
1
11

FIG. 8

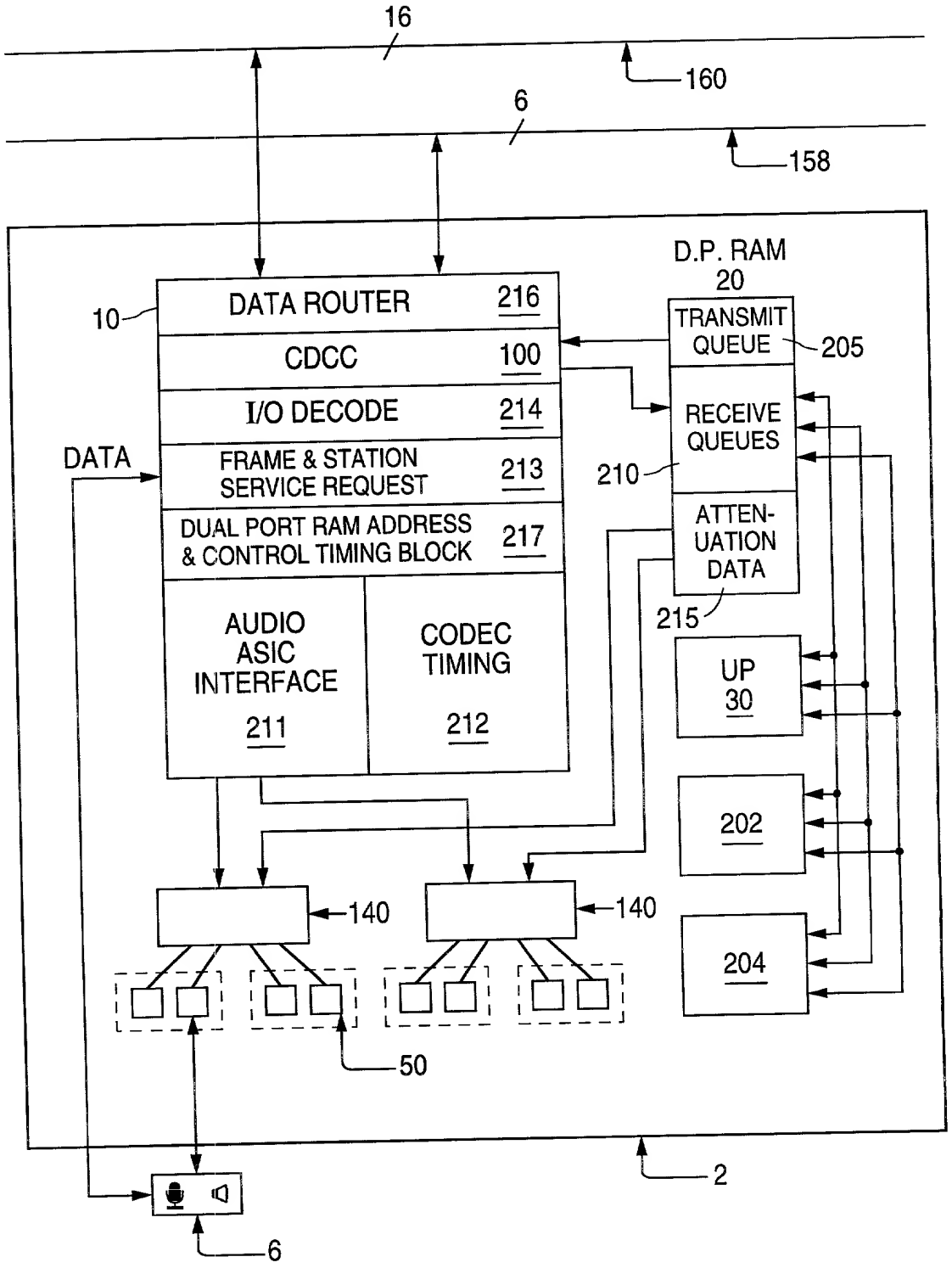
16
160
6
158
D.P. RAM
20
10
DATA ROUTER
216
CDCC
100
I/O DECODE
214
FRAME & STATION
SERVICE REQUEST
213
DUAL PORT RAM ADDRESS
& CONTROL TIMING BLOCK
217
AUDIO
ASIC
INTERFACE
211
CODEC
TIMING
212
DATA
TRANSMIT
QUEUE
205
RECEIVE
QUEUES
210
ATTEN-
UATION
DATA
215
UP
30
202
204
140
140
50
2
6

FIG. 2

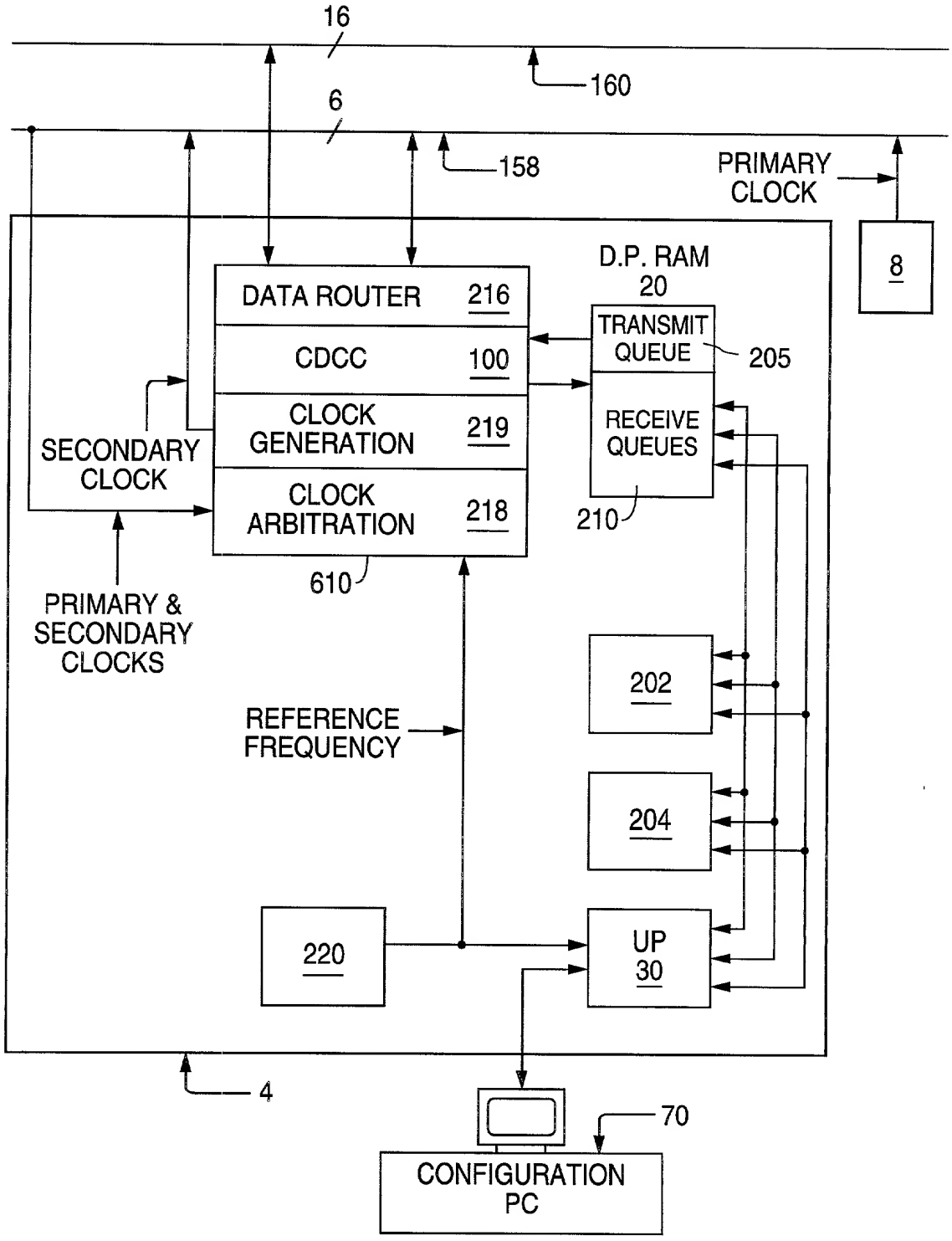
16
160
6
158
PRIMARY CLOCK
8
D.P. RAM 20
DATA ROUTER 216
CDCC 100
CLOCK GENERATION 219
CLOCK ARBITRATION 218
TRANSMIT QUEUE
205
RECEIVE QUEUES
210
SECONDARY CLOCK
610
PRIMARY & SECONDARY CLOCKS
REFERENCE FREQUENCY
202
204
220
UP 30
4
70
CONFIGURATION PC

FIG. 3

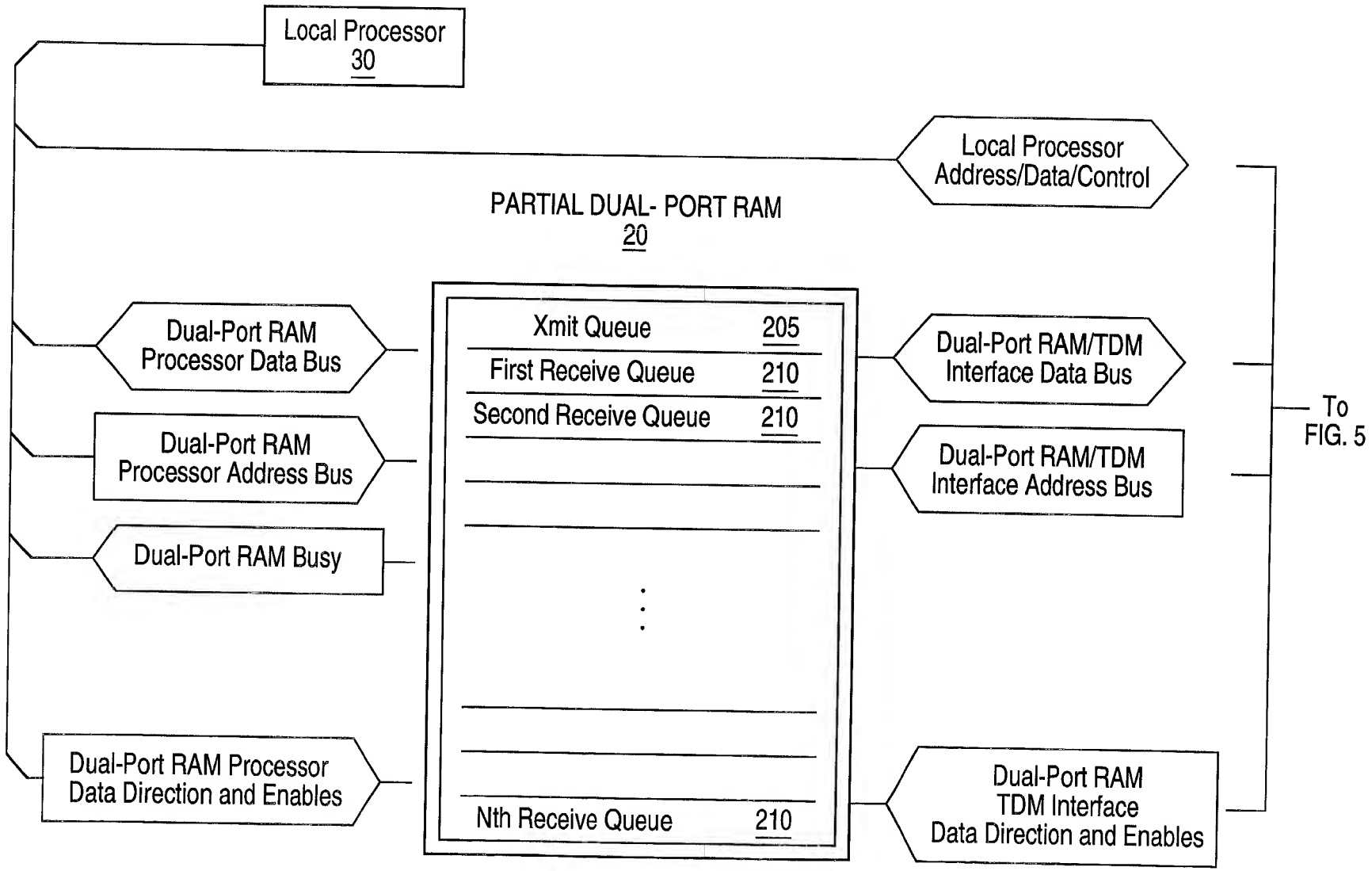

FIG. 4

FIG. 5

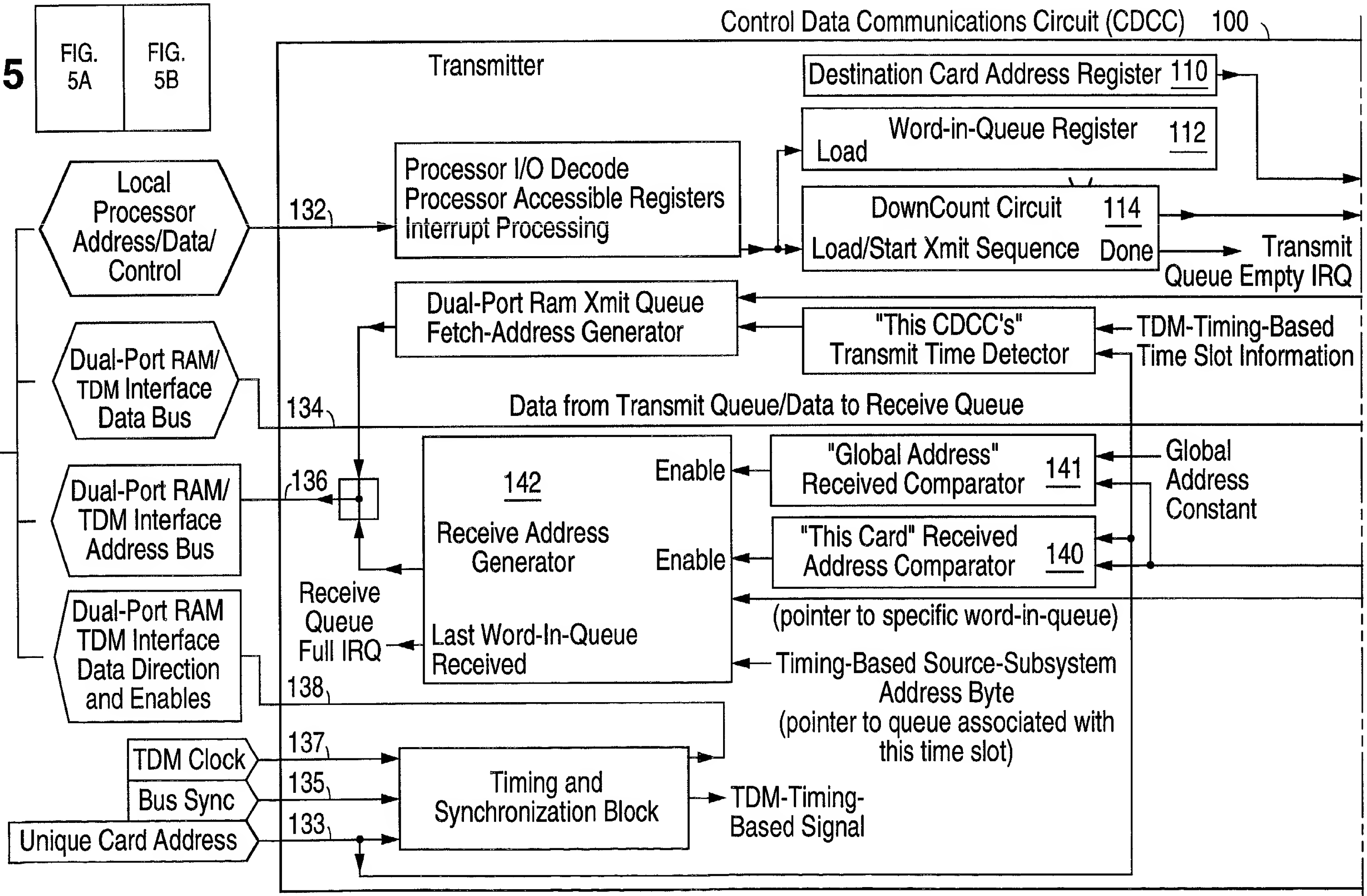
FIG. 5A
FIG. 5B
Control Data Communications Circuit (CDCC) 100
Transmitter
Destination Card Address Register 110
Word-in-Queue Register 112
Load
DownCount Circuit 114
Load/Start Xmit Sequence
Done
Transmit Queue Empty IRQ
Local Processor Address/Data/ Control
132
Processor I/O Decode
Processor Accessible Registers
Interrupt Processing
Dual-Port Ram Xmit Queue Fetch-Address Generator
"This CDCC's" Transmit Time Detector
TDM-Timing-Based Time Slot Information
Dual-Port RAM/ TDM Interface Data Bus
134
Data from Transmit Queue/Data to Receive Queue
To FIG. 4
Dual-Port RAM/ TDM Interface Address Bus
136
142
Receive Address Generator
Enable
Enable
"Global Address" Received Comparator 141
"This Card" Received Address Comparator 140
Global Address Constant
(pointer to specific word-in-queue)
Receive Queue Full IRQ
Last Word-In-Queue Received
Timing-Based Source-Subsystem Address Byte
(pointer to queue associated with this time slot)
Dual-Port RAM TDM Interface Data Direction and Enables
138
TDM Clock
137
Bus Sync
135
Unique Card Address
133
Timing and Synchronization Block
TDM-Timing-Based Signal

FIG. 5A

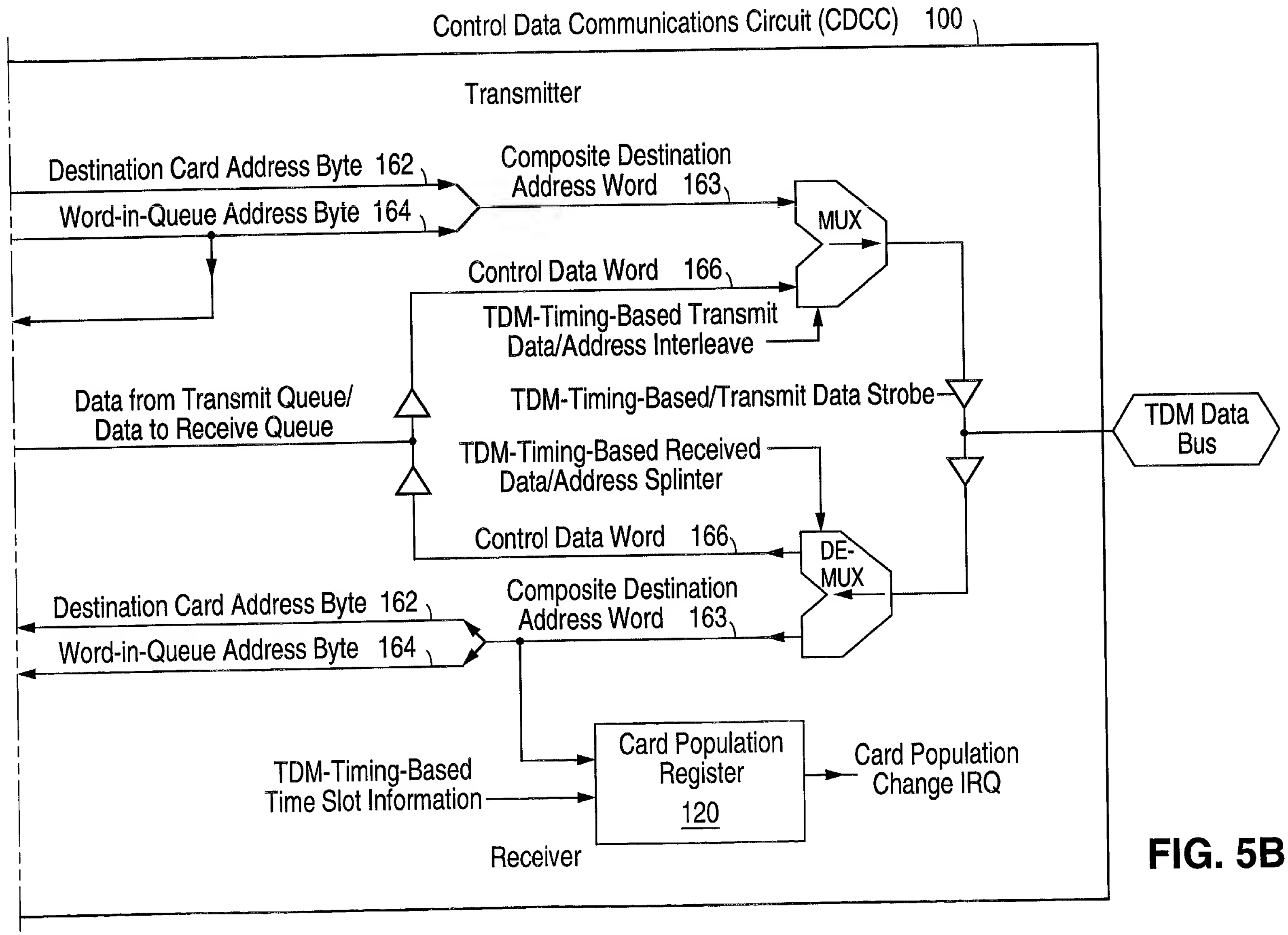
Control Data Communications Circuit (CDCC) 100
Transmitter
Destination Card Address Byte 162
Word-in-Queue Address Byte 164
Composite Destination Address Word 163
MUX
Control Data Word 166
TDM-Timing-Based Transmit Data/Address Interleave
Data from Transmit Queue/ Data to Receive Queue
TDM-Timing-Based/Transmit Data Strobe
TDM Data Bus
TDM-Timing-Based Received Data/Address Splinter
Control Data Word 166
DE-MUX
Destination Card Address Byte 162
Word-in-Queue Address Byte 164
Composite Destination Address Word 163
Card Population Register
120
Card Population Change IRQ
TDM-Timing-Based Time Slot Information
Receiver

FIG. 5B

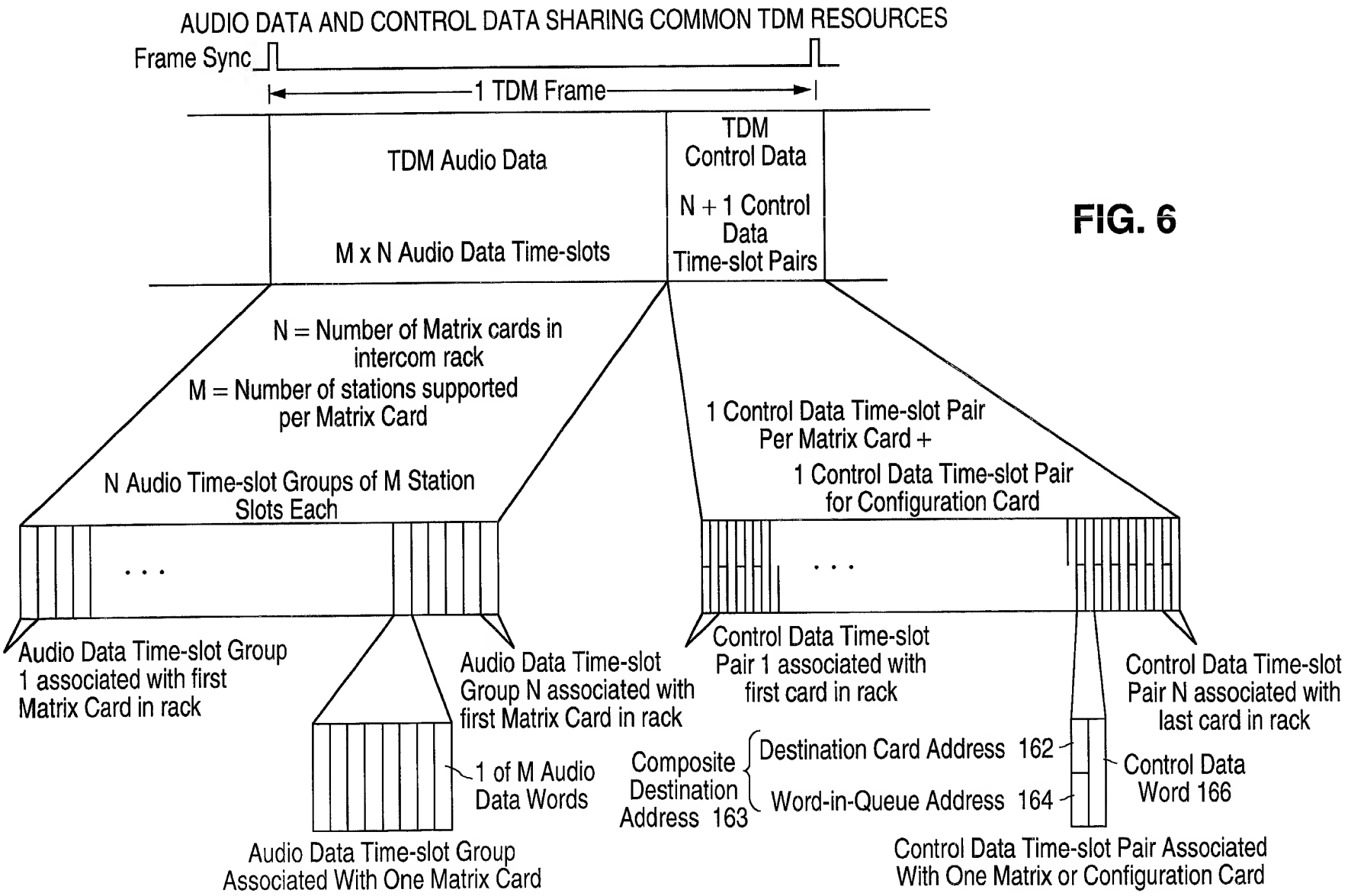
AUDIO DATA AND CONTROL DATA SHARING COMMON TDM RESOURCES
Frame Sync
1 TDM Frame
TDM Audio Data
M x N Audio Data Time-slots
TDM Control Data
N + 1 Control Data Time-slot Pairs
N = Number of Matrix cards in intercom rack
M = Number of stations supported per Matrix Card
N Audio Time-slot Groups of M Station Slots Each
1 Control Data Time-slot Pair Per Matrix Card +
1 Control Data Time-slot Pair for Configuration Card
Audio Data Time-slot Group 1 associated with first Matrix Card in rack
Audio Data Time-slot Group N associated with first Matrix Card in rack
Control Data Time-slot Pair 1 associated with first card in rack
Control Data Time-slot Pair N associated with last card in rack
1 of M Audio Data Words
Composite Destination Address 163
Destination Card Address 162
Word-in-Queue Address 164
Control Data Word 166
Audio Data Time-slot Group Associated With One Matrix Card
Control Data Time-slot Pair Associated With One Matrix or Configuration Card

FIG. 6

Attorney's Docket No. 20583.00110 - PATENT

COMBINED DECLARATION FOR PATENT APPLICATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

INTERCOM SYSTEM HAVING UNIFIED CONTROL AND AUDIO DATA TRANSPORT

the specification of which (check one) _ is attached hereto or X was filed on April 7, 1997 as Application Serial No. 08/835,339 and was amended on (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed Yes	No
Number	Country	Day/Month/Year Filed		

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

60/042,965	April 4, 1997	Pending
Application Ser. No.	Filing Date	Status: Patented, Pending, Abandoned

I HEREBY APPOINT THE FOLLOWING AS MY ATTORNEYS WITH FULL POWER OF SUBSTITUTION TO PROSECUTE THIS APPLICATION AND TRANSACT ALL BUSINESS IN THE PATENT OFFICE CONNECTED THEREWITH: Malcolm B. Wittenberg, Registration No. 27,028, Nathan P. Koenig, Registration No. 38,210, Adam H. Tachner, Registration No. 40,343, and Vincent E. Duffy, Registration No. 39,964.

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Inventor's signature _____ 11/17/97
Date

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Citizenship U.S.A.

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